IMPLANTED ASYMMETRIC DOPED POLYSILICON GATE FinFET

Abstract of the Disclosure

An asymmetric field effect transistor (FET) that has a threshold voltage that is compatible with current CMOS circuit designs and a low-resistance gate electrode is provided. Specifically, the asymmetric FET includes a p-type gate portion and an n-type gate portion on a vertical semiconductor body; an interconnect between the p-type gate portion and the n-type gate portion; and a planarizing structure above the interconnect.

Figures